Claims:

1. A method of implementing the Viterbi algorithm comprising:

calculating branch metrics for branches of the Viterbi trellis;

combining branch metrics with old path metrics to produce candidate path metrics;

selecting a new path metric associated with a selected trellis path for each state in trellis from the candidate path metrics;

composing an optimal path value for each state in trellis, the optimal path value indicating multiple transitions of the selected trellis path.

2. The method of Claim 1 wherein the optimal path value is comprised of optimal path value fragments

3. The method of Claim 2 wherein the optimal path value fragments are stored in memory blocks.

4. The method of Claim 1 further comprising using the optimal path value to determine an output value.

5. The method of Claim 4 wherein the optimal path value for the lowest state of the Viterbi trellis at the end of a block of symbols indicates the transmitted symbols in the block.

6. The method of Claim 4, wherein the optimal path value for state zero indicates the transmitted symbols in a block of symbols.

7. The method of Claim 1 wherein the new data added to the optimal path indicates a new decoded bit.

8. The method of Claim 1 wherein the new data is a new data bit.

9. The method of Claim 1 wherein a traceback pointer is used to select between two prior optimal path values.

10. The method of Claim 9 wherein the old optimal path values are selected
from optimal path values for states that can transition into current state.

11. The method of Claim 9 wherein the new data is added to the selected optimal path value of the prior state.

12. The method of Claim 1 wherein the Viterbi algorithm is implemented in a reconfigurable chip.

13. The method of Claim 1 wherein the new path metric selecting and optimal path value composing steps operate in parallel.

14. An apparatus to implement the Viterbi algorithm comprising:

a path metric storage adapted to store a path metric associated with a selected trellis path for each state in the Viterbi trellis;

a path update unit adapted to update each path metric;

an optimal path value storage adapted to store an optimal path value for each state in trellis, the optimal path value indicating multiple transitions of the selected trellis path; and

a optimal path value update unit adapted to update each optimal path value.

15. The apparatus of Claim 14 further comprising an output unit adapted to use an optimal path value to determine an output value.

16. The apparatus of Claim 15 wherein the output value produces the optimal path value for the state with the lowest path metric.

17. The apparatus of Claim 14 wherein the updating of multiple states, path metrics and optimal path value are done at the same time.

18. The apparatus of Claim 14 wherein the path metric update and optimal path value update operates in parallel.

19. The apparatus of Claim 14 implemented on reconfigurable logic.

20. The apparatus of Claim 19 wherein the optimal path updating uses resources not required for the path metric update unit.

21. The apparatus of Claim 14 wherein no serial traceback operation is required.

22. The apparatus of Claim 14 wherein the optimal path value storage is separated into multiple memory blocks.

23. The apparatus of Claim 22 wherein the optimal path value comprises optimal path fragments stored in the memory blocks.

24. The apparatus of Claim 23 wherein the optimal path value updating unit operates on optimal path value fragments to update the optimal path value.

25. The apparatus of Claim 23 wherein, during the readback operation, the optimal path fragment from one memory block is used to determine a pointer to an optimal path fragment in another memory block.